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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,263	11/17/2003	Narain D. Arora	SIPRP101US	4577
23623	7590	12/22/2005	EXAMINER	
AMIN & TUROCY, LLP 1900 EAST 9TH STREET, NATIONAL CITY CENTER 24TH FLOOR, CLEVELAND, OH 44114			NGUYEN, JIMMY	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 12/22/2005 .

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

**Office Action Summary**

Application No.

10/715,263

Applicant(s)

ARORA ET AL

Examiner

Jimmy Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
 Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 13 October 2005.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 - 45 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 - 36, 39 - 45 is/are rejected.
- 7) ☒ Claim(s) 37 and 38 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
 Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### **Response to Argument**

The examiner acknowledges the amendment filed 10/13/05 with the following effect;

The applicants argue that the examiner is employing a 20/20 hindsight road map based analysis to impermissibly provide the missing teaching of the cited document. In essence, the examiner is basing the rejection on an assertion that it would have been obvious to do something not suggested in the art based on the advantages disclosed in applicants' specification. The examiner is respectfully traverse this argument. Based on MPEP section 2100 a prima facie case of obviousness will establish against applicants' claimed invention when there is a " duplication of the essential working parts of a device involves".

As explained in detail above, the amendments do not render the claims distinct and patentable over prior art; nor do the amendments overcome the rejection. The applicant's arguments have considered in full, but they are deemed to be unpersuasive. Therefore, this final rejection is made.

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 -36, 39 - 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bourgoin et al (US 5,804,709)

**As to claims 1,29, 32, 43, 44**, Bourgoin et al disclose (figs 2 – 4) a system and a method that facilitates non-invasive in-line characterization of parameters of VLSI circuit interconnects, comprising:

A voltage source (Vdc) the outputs a plurality of disparate voltages;  
a of micro-electro-mechanical system (MEMS, 320) cantilevers that apply voltage to VLSI circuit (231, fig 2A) interconnect without physical contact thereto;  
a measuring component ( column 9 and 10) that measures deflection characteristics of the cantilevers,  
the deflections correspond to electrical forces generated from the applied voltages (Vdc) as passed through VLSI circuit (231) interconnect and  
a component that computes characteristics of the VLSI interconnect ( **claim 1, measure a characteristic of the sample**) based at least in part upon the measured deflection characteristics.

However, Bourgoin et al disclose only one (MEMS, 320). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide the additional MEMS, 320 since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art, St. Regis Paper Co.v. Bemis Co., 193 USPQ 8.

**As to claim 2**, Borgoin et al disclose (figs 2 – 4) the system further comprising a control component (372) that effectuates control of a VLSI circuit fabrication process step based at least in part upon the computed characteristics.

**As to claim 3**, Borgoin et al disclose (figs 2 – 4) the system further comprising the computed characteristics are employed as feedback (470) information to the control component.

**As to claim 4**, Borgoin et al disclose (figs 2 – 4) the system further comprising the computed characteristics are employed as feed forward information to the control component.

**As to claim 5**, Borgoin et al disclose (figs 2 – 4) the MEMS cantilevers comprise conductive tips (321) to effectuate injection of voltages into the VLSI circuit components.

**As to claim 6**, Borgoin et al disclose (figs 2 – 4) the MEMS cantilever (320) act as a conductive path to the conductive tips (321).

**As to claim 7**, Borgoin et al disclose (figs 2 – 4) the system wherein a conductive path is provided on the MEMS cantilevers (320) to the conductive tips to facilitate injection of currents into the VLSI circuit interconnects.

**As to claim 8**, Borgoin et al disclose (figs 2 – 4) the test structure for capacitance and/or resistance measurement. (claim 1, measuring characteristic of a sample).

**As to claim 9**, Borgoin et al disclose (figs 2 – 4) the system of claim 1, further comprising a voltage source ( $V_{dc}$ ) that delivers voltages to the MEMS cantilevers (320) the voltage source delivering disparate voltages to disparate MEMS cantilevers.

**As to claim 10**, Borgoin et al disclose (figs 2 – 4) the system wherein the measuring component comprising photo-detector (or antenna, 361) that detects a laser beam (323) deflecting off at least one MEMS cantilever (320).

**As to claim 11**, Borgoin et al disclose (figs 2 – 4) the measuring component comprises an optical interferometer.

**As to claims 12, 13,** Borgoin et al disclose (figs 2 – 4) the system further comprising a positioning component (scanner) that facilitates proper positioning of the MEMS cantilevers with respect to the VLSI circuit interconnect.

**As to claims 14,15,** Borgoin et al disclose (figs 2 – 4) the system further comprising a pre-amplifier and amplifier (462).

**As to claims 16 - 19,** Borgoin et al disclose (figs 2 – 4) the system further comprising a tuning fork, wherein at least one MEMS cantilever (320) is attached to the tuning fork.

**As to claim 20,** Borgoin et al disclose (figs 2 – 4) the system at least one MEMS cantilever is a piezo-resistive cantilever (320).

**As to claims 21, 22,** Borgoin et al disclose (figs 2 – 4) the system employed to measure coupling capacitance between VLSI circuit interconnects and measure capacitance between VISI circuit and ground plane (claim 1, measure electrical characteristic).

**As to claim 23,** Borgoin et al disclose (figs 2 – 4) the MEMS cantilevers (420) and the VLSI circuit interconnects are within a vacuum chamber (491).

**As to claims 24, 42,** Borgoin et al disclose (figs 2 – 4) the system utilized to characterize at least one of resistance and capacitance of a transistor (441).

**As to claims 25, 26,** Borgoin et al disclose (figs 2 – 4) a distance between VLSI circuit interconnects is less than 0.2 micron and a length of VLSI is less than 10 micron (this is an optimum value of a result effective variable involves only routine skill in the art).

**As to claims 27, 28,** Borgoin et al disclose (figs 2 – 4) the system wherein at least a portion of a first VLSI circuit interconnect to be tested is on a disparate layer compared to a second VLSI circuit interconnect to be tested and the VLSI circuit interconnects are covered by a layer of dielectric.

**As to claims 30, 31,** Borgoin et al disclose (figs 2 – 4) the system wherein the computing component calculates a coupling capacitance between VLSI circuit interconnects based at least in part upon the measured deflection characteristics and computing component calculates a capacitance of a VLSI circuit interconnect that is not contact by the first MEMS cantilever with respect to ground.

**As to claims 33, 34, 41, 45,** Borgoin et al disclose (figs 2 – 4) the method further comprising computing coupling capacitance between the two adjacent VLSI circuit interconnects based at least in part upon the measured oscillations

**As to claims 35, 36, 39, 40,** Borgoin et al disclose (figs 2 – 4) the method further comprising:

Providing a first voltage to a first MEMS cantilever (420) with a frequency substantially similar to one half of at least one of natural resonant frequency and a user selected frequency of the first MEMS cantilever and  
Grounding a second MEMS cantilever.

***Allowable Subject Matter***

3. Claims 37, 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior arts of record are fail to disclose the combination of the based claims with providing a first voltage to a first MEMS cantilever with a frequency substantially similar to  $b f_{res6}$  where  $b$  is a constant such that  $b \geq 1.3$  and resonance frequency ( $f_{res6}$ ) is substantially similar to one half of at least one of a resonant frequency and a user selected frequency of a second MEMS cantilever; and

Providing a second voltage to the second MEMS cantilever with a frequency substantially similar to  $f_{res}(1 + ab)$  where  $a$  resonance frequency( $f_{res5}$  is substantially

similar to half a resonant frequency of the first MEMS cantilever a is substantially similar to fres5/fres6

### **Conclusion**

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen whose telephone number is 571-272-1965. The examiner can normally be reached on M-F from 9 to 5.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ramtez Nestor, can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jimmy Nguyen

12/16/05

  
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12/20/05